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A SIMULATION STUDY OF SHORT CHANNEL EFFECTS IN CONVENTIONAL AND LIGHTLY-DOPED-DRAIN (LDD) P-MOSFETS

N. SOIN, D. ABD HADI

Department of Electrical Engineering, Faculty of Engineering, University of Malaya, Kuala Lumpur, Malaysia

Abstract This paper presents the comparative study of the short channel effects on both conventional and lightly doped drain (LDD) pMOSFETs. This includes the parametric study of both structures in order to determine the profile of the threshold voltage and leakage current due to the short channel effects. In this study, two critical parameters of the short channel devices were investigated including the channel length (L) and the oxide thickness (T_{ox}). The significant effects were observed in the device especially on the leakage current mechanism includes substrate and drain currents when these two critical parameters have been scaled down. Apart from that, the influence of device processing parameter namely, source/drain ion implantation dose on the leakage current mechanism had been investigated

KEYWORDS: Short channel effects, leakage current, PMOSFET, Lightly doped drain, channel length, oxide thickness

Introduction

Reliability of deep submicrometer for *n* and *p* channel MOSFET's is a mandatory issue for device scaling and much effort had been made to investigate device degradation (Kaga, 1988). Most of the studies focus on NMOSFETs since the short channel effects are said to be more significant in that particular device compared to PMOSFETs due to larger ionization of electrons in NMOSFET than holes in PMOSFETs (Picher *et al.*, 1999). However, the hot carrier degradation has to be taken into account for PMOSFET with a submicrometer channel length (Picher *et al.*, 1999). The main purpose of this study is to compare the short channel effects on both conventional and LDD PMOSFETs and investigate the capability of the LDD PMOSFET structure in reducing these effects in terms of leakage current and threshold voltage.

Simulation and Device Conditions

Simulation study of short channel effects on the conventional and Lightly Doped Drain (LDD) PMOSFET structures has been conducted using MINIMOS 6.1 (Picher *et al.*, 1999). The 2-D and AVAL models from MINIMOS 6.1 have been used in this simulation. The features of the simulated LDD PMOSFET structure are listed below:

- Gate Oxide : 5.5×10^{-7} cm
- Gate Material : p-doped polysilicon (0.55 V)
- Channel Width : 1.0×10^{-4} cm
- Channel Implantation : Arsenic, 1.7×10^{12} cm $^{-2}$, 10 keV
  : Arsenic, 8.0×10^{12} cm $^{-2}$, 35 keV

Correspondence: Norhayati Soin, Department of Electrical Engineering, Faculty of Engineering, University of Malaya, Kuala Lumpur, Malaysia

- Source/Drain Doping Profile
  : p^+ region; Boron, 8.0×10^{15} cm $^{-2}$, 95 keV, , XOFF = 50.0×10^{-7} cm
  : p^- region; Boron, 7.0×10^{14} cm $^{-2}$, 20 keV
  : Bulk Doping; 1.0×10^{16} cm $^{-3}$

To simulate the conventional PMOSFET structure, the features are the same except for the non-existing of p^- region in the simulated device. Two biased conditions have been considered in this study as stated below:

i. Condition I: $V_G = -2.0$ V and $V_D = -0.1$ V
ii. Condition II: $V_G = -2.5$ V and $V_D = -5.0$ V

In both conditions, the source and substrate were connected to the ground.

Results and Discussion

It was found that as the channel length decreased from 1 μm to 0.18 μm, the drain current increased for both conventional and LDD structures as shown in Figure 1. By comparing the amount of drain current, it was found that the LDD structure managed to reduce the short channel effects compared to the conventional structure since the amount of the drain current for LDD was less than the conventional structure. This is because of the lightly doped regions in the LDD structure in which the magnitude of the electric field at the oxide-semiconductor interface is less than in the conventional structure as shown in Fig. 2. This phenomenon is clearly described in Fig. 2 which shows the physical geometries of a conventional n^+ drain contact and LDD structure superimposed on the same plot.

Besides, the lightly doped regions can contribute to an additional mechanism to the difference between sources and drain resistances (R_d-R_s) and also can increase effective channel of the LDD MOSFET device (Md. Rofiqul Hassan *et al.*, 1997). The (R_d-R_s) value can be obtained by the given equation [1]:

$$(R_d - R_s) = \frac{V_{gi} - V_{gn}}{I_D\left(1 + \frac{dV_T}{dV_{SB}}\right)} \quad \text{..... (1)}$$

where, V_{gn} and V_{gi} are the intrinsic gate-source voltages in the normal and inverse mode respectively. The term dV_T/dV_{SB} accounts for the dependence of the threshold voltage with respect to the body voltage, V_{SB}. From equation (1) it clearly shows that the relationship between (R_d-R_s) and the drain current, I_D whereas the (R_d-R_s) is inversely proportional to I_D. As (R_d-R_s) is increased in the LDD PMOSFET, the drain current will decrease due to the presence of the lightly doped regions that has been introduced to the (R_d-R_s). This is one of the reasons that explain the result as shown in Fig. 1.For the LDD PMOSFET, it can be seen that the drain and substrate currents decreased as compared to that of the conventional structure.

Several studies have found out that by scaling down the channel length, the oxide thickness will simultaneously be scaled (Young Jin Choi, 1998; Richard C. Jaeger, 2002). Another conclusion made from the previous study stated that the oxide thickness is strongly dependent on the threshold voltage for both structures (Conventional PMOSFET and LDD PMOSFET), especially for the LDD PMOSFET structure (Md. Rofiqul Hassan *et al.*, 1997). Figure 3 shows that for both structures, the trend of V_{TH} versus T_{ox} is very similar except for their magnitudes. It can be seen from Fig. 3 that the threshold voltage of the LDD PMOSFET is less than the threshold voltage of the conventional structure. This is due to the threshold voltage that is determined from the inversion mechanism in the n-type substrate, but not from the make up of the drain and source region (Young Jin Choi, 1998).

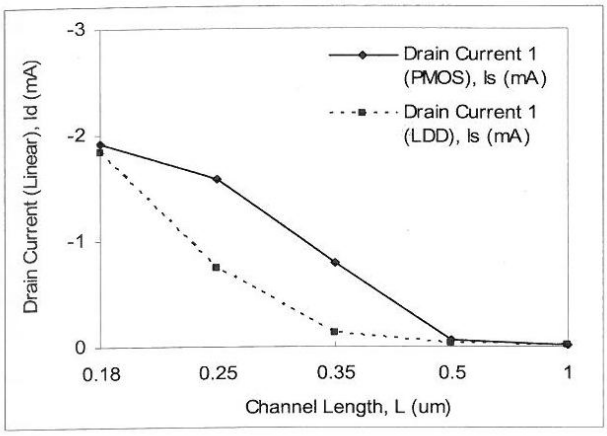

Figure 1. The graph of linear drain current versus channel length when $T_{ox} = 2$ nm

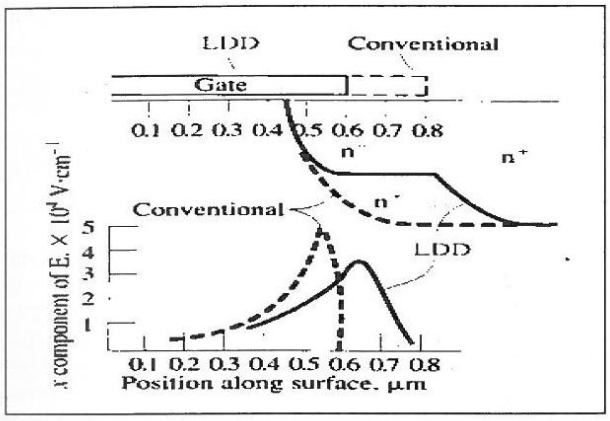

Figure 2. Magnitude of the electric field at the Si-SiO_2 interface as a function of distance

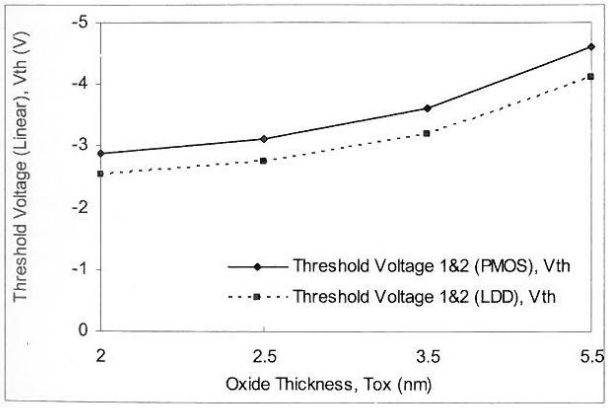

Figure 3. Graph of threshold voltage versus oxide thickness for both structures

Conclusion

Overall, it was found that the LDD PMOSFET effectively reduced the electric field near the drain region and consequently minimized leakage current such as substrate currents. Besides, the LDD structure also improved the threshold voltage in such device.

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